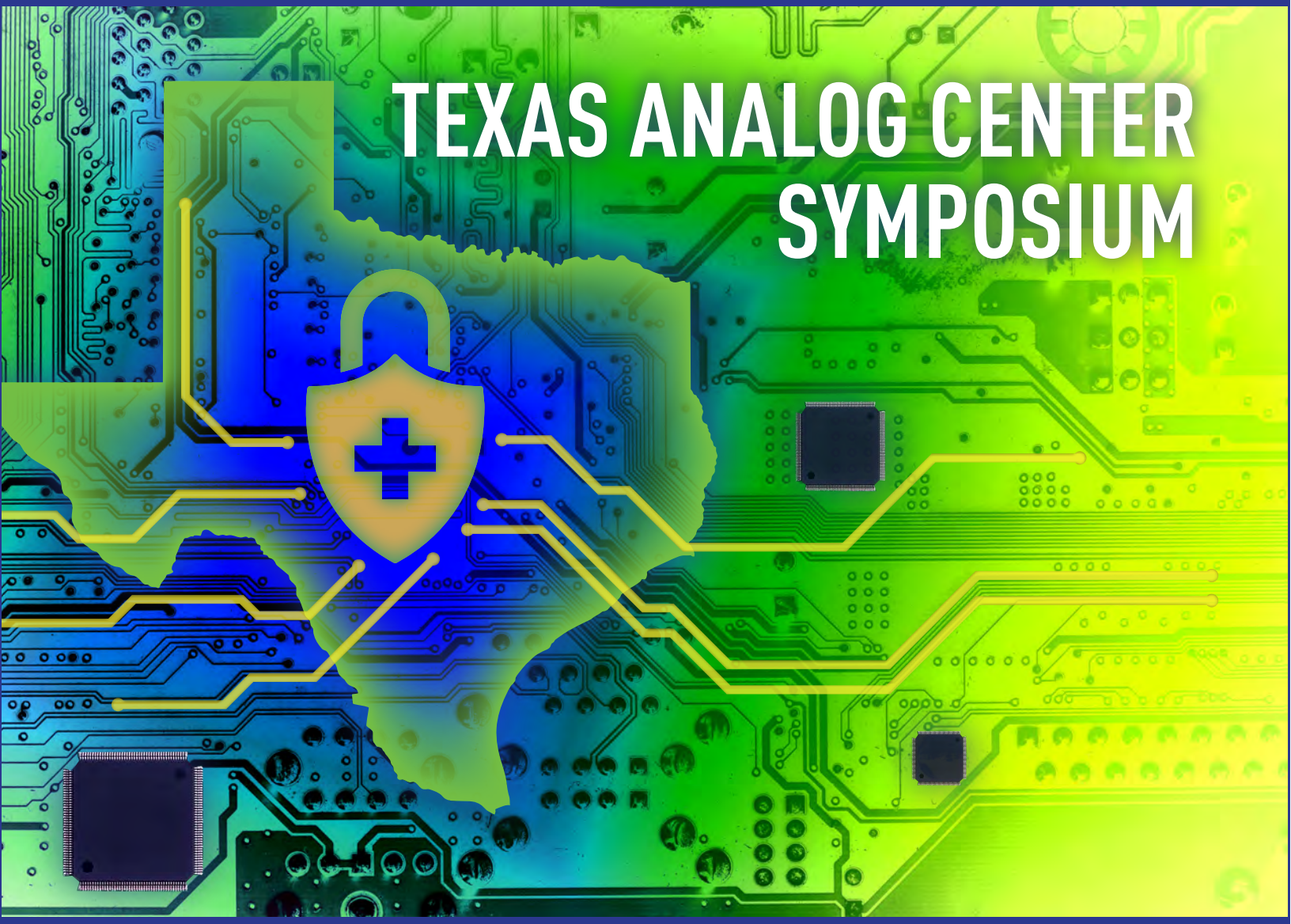
TXACE TEXAS ANALOG CENTER OF EXCELLENCE



TEXAS ANALOG CENTER SYMPOSIUM

October 17, 2022

THE UNIVERSITY OF TEXAS AT DALLAS
ERIK JONSSON SCHOOL OF ENGINEERING AND COMPUTER SCIENCE

TEXAS ANALOG CENTER OF EXCELLENCE
SYMPOSIUM

Symposium Chair: Yiorgos Makris
Poster Session Chairs:
Naofal Al-Dhahir, Kanad Basu and Sam Shichijo

October 17, 2022

MORNING SESSION 8:30 a.m. – 12:10 p.m. CDT

8:30 a.m.	**Registration and Morning Refreshments**
9 a.m.	**Symposium Opening:** Yiorgos Makris - Professor, UT Dallas
9:10 a.m.	**Keynote Speaker:** *(Un)Intended Communications* James Wilson - Program Manager, DARPA
9:55 a.m.	**Keynote Speaker:** *AI and the Path to an Autonomous Future* Dave Copps - CEO, Worlds
10:40 a.m.	**Coffee Break**
10:50 a.m.	**Panel:** *When Will My Car Drive Me to Work?* Moderated by Ali Niknejad - Professor, University of California, Berkeley

LUNCH 12:10 p.m. – 1:15 p.m. CDT

12:30 p.m.	**Lunch Talk:** *Going Full Circle From Academia to Startup, Exit, and Then Back at it Again* Arjang Hassibi - Co-Founder and CEO, Siomyx Inc.

AFTERNOON SESSION 1:20 p.m. – 4:40 p.m. CDT

1:20 p.m.	**Students Poster Previews**
2 p.m.	**Poster Session**
3:20 p.m.	**Invited Speakers:** *Mars Helicopter Communication Link and Innovative Antenna for Cubesats, Landers and Rovers* Gaurangi Gupta (Presenter) - Post Doctoral Researcher, Jet Propulsion Laboratory Nacer Chahat - Senior Antenna/Microwave Engineer, Jet Propulsion Laboratory
4:05 p.m.	**Center Overview:** Ken K. O - Director of TxACE and Professor, Texas Instruments Distinguished University Chair, UT Dallas
4:20 p.m.	**Student Poster Awards and Closing Remarks:** Sam Shichijo and Ken K. O

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9 a.m. CDT

Yiorgos Makris
Professor, The Jonsson School
The University of Texas at Dallas

Symposium Opening

BIO: Yiorgos Makris received the Diploma of Computer Engineering and Informatics from the University of Patras, Greece, in 1995 and the MS and PhD degrees in computer engineering from the University of California, San Diego, in 1998 and 2001, respectively. After spending a decade on the faculty of Yale University, he joined UT Dallas where he is now a professor of electrical and computer engineering, director of the Trusted and RELiable Architectures (TRELA) Research Laboratory, co-founder and site-PI of the NSF Industry-University Cooperative Research Center on Hardware and Embedded System Security and Trust (NSF CHEST I/UCRC), as well as leader of the Safety, Security and Healthcare Thrust of the Texas Analog Center of Excellence (TxACE). His research focuses on applications of machine learning and statistical analysis in the development of trusted and reliable integrated circuits and systems, with particular emphasis on the analog/RF domain. He also investigates hardware-based malware detection, forensics and reliability in microprocessors, security primitives in synthetic biology, as well as on-die learning and novel computational modalities using emerging technologies. His research activities have been supported by NSF, SRC, ARO, AFRL, AFWERX, DARPA, DoE/Honeywell, Boeing, Northrop Grumman, KBR/Wyle, IBM, LSI, Intel, AMS, Advantest, Qualcomm and TI. He has served as an associate or guest editor for the IEEE Transactions on Information Forensics and Security, the IEEE Transactions on Computers, the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems and the IEEE Design & Test periodical. He is a Senior Member of the IEEE, a recipient of the 2006 Sheffield Distinguished Teaching Award, a recipient of the Best Paper Award from the 2013 Design Automation and Test in Europe (DATE'13) conference and the 2015 VLSI Test Symposium (VTS'15), a recipient of the Best Hardware Demonstration Award from the 2016 and 2018 Symposia on Hardware Oriented Security and Trust (HOST'16 and HOST'18) and a recipient of the 2020 Faculty Research Award from the Erik Jonsson School of Engineering and Computer Science at UT Dallas.

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9:10 a.m. CDT

James Wilson
Program Manager
Microsystems Technology Office (MTO)
DARPA

(Un)Intended Communications

ABSTRACT: "(Un)Intended Communications" will provide a brief introduction to the Microsystems Technology Office (MTO) at DARPA, then dive into the two sides of communication: intended communication and unintended communication. Several programs that MTO has had or are currently running in the commination area will be highlighted, including MAX, SPiNN, MIDAS and WiSPER. Then the focus switches to unintended communications with a brief overview of MTO hardware security. The seminar will conclude with a new research area focused on the missing piece of the hardware security problem.

BIO: James Wilson joined DARPA in July 2020 as a program manager in the Microsystems Technology Office (MTO). His research interests include the development of radio frequency (RF), analog, and digital circuits that push the power and performance envelope; novel topologies enabled through heterogeneous integration; the applications of electronics to enable new RF, EW, and communication opportunities; and hardware security. He is particularly interested in increasing the energy efficiency of electronics to enable ubiquitous, high-performance systems for wideband electromagnetic spectrum operations. Before joining DARPA, Wilson was a team leader of the Silicon Design Team at the Army Research Laboratory (ARL). In this role, he led technology and program development in the area of microsystem technology, which spans analog, RF and digital circuit and system design for a wide variety of applications, including communications, radar, electronic support and remote sensing. In his first six years at ARL as an electronics engineer, he developed digital-to-analog converters and radio frequency integrated circuits (RFIC) frontends using advanced CMOS and heterogeneous technologies. Wilson holds bachelor's, master's, and PhD degrees in electrical engineering from The Ohio State University, and has published more than 20 papers. He is a senior member of the IEEE and served for five years on the technical program committee of the RFIC Symposium. He also served on the steering committee of the GOMACTech Conference since 2012 and was the general chair of the conference in 2016.

9:55 a.m. CDT

Dave Copps
CEO
Worlds

AI and the Path to an Autonomous Future

ABSTRACT: Building automation into the real world has rapidly moved from a good idea to what's next in the evolution of AI. Whether it involves navigating autonomous vehicles or building the industrial metaverse, organizations all over the world are now focusing on how they can radically increase their levels of AI-based automation. Through unique combinations of sensors, digital twins and AI, we are not only digitizing and dematerializing the real world but enabling entirely new possibilities in how we can accelerate and automate it.

BIO: Dave Copps is known locally and internationally as a futurist, technologist and visionary regarding the roles that emerging technologies will play in transforming markets and the world. Dave Copps has founded, launched and sold two technology companies that have placed machine learning and artificial intelligence in hundreds of companies around the world. In 2017 Copps was recognized as Emerging Company CEO of the Year in Texas while serving as CEO of Brainspace Corporation which was acquired by Cyxtera in 2017. Copps received his BA from the University of North Texas. He is an invited member of the Aspen Institute's Roundtable on AI, a frequent speaker at MIT's EmTech conferences as well as universities and technology incubators all over the world including Capital Factory, Health Wildcatters and the Dallas Entrepreneurs Center (The DEC) in his home town of Dallas, Texas.

When Copps is not being a geek, he enjoys collecting custom guitars and exotic cars, brewing craft beer, ocean sailing and family time at his home on the island of Bequia in the Caribbean.

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PANEL: When Will My Car Drive Me to Work?

10:50 a.m. CDT

PANEL ABSTRACT: Everyone loves a thrilling drive, but commuting to work in crawling stop-and-go traffic is no fun at all. Wouldn't you rather get some work done or read a nice book? Well, soon you will have this option. How soon? This panel seeks to answer this very question by examining the key technological advances needed to make truly autonomous "level 5" driving possible. The panel of experts will discuss limitations and key innovations needed to enable truly driverless vehicles. This panel will answer several questions, including the need for 3D imaging/sensing. In particular, is LiDAR technology sufficient or can MIMO mm-wave radar fulfill all the needs for detection of the environment? Will these vehicles require a "5G" low latency connection to assist with traffic flow and higher-level traffic alerts? Is vehicle-to-vehicle (V2V) communication necessary? What are the key algorithms and signal processing and AI/ML computation requirements, and when will they be cost and power efficient enough to be put into commercial vehicles? Finally, what's the business model that could potentially unlock this technology, such as ride-share services?

Organizer

Ali M. Niknejad
Professor
University of California, Berkeley

BIO: Ali M. Niknejad (Fellow, IEEE) received a BS degree in electrical engineering from the University of California at Los Angeles in 1994 and MS and PhD degrees in electrical engineering from the University of California at Berkeley in 1997 and 2000, respectively. He is currently a professor with the EECS Department at UC Berkeley, the faculty director of the Berkeley Wireless Research Center (BWRC) and the associate director of the ComSenTer, a multi-university center for converged terahertz communications and sensing. His research interests lie within the area of wireless and broadband communications and biomedical imaging and sensors, integrated circuit technology (analog, RF, mixed-signal, and mm-wave), device physics and compact modeling, and applied electromagnetics. Niknejad and his coauthors received the 2017 IEEE Transactions on Circuits and Systems Darlington Best Paper Award, the 2017 Most Frequently Cited Paper Award from 2010 to 2016 at the Symposium on VLSI Circuits, the CICC 2015 Best Invited Paper Award and the 2014 VLSI Best Paper Award. He was a recipient of the 2012 ASEE Frederick Emmons Terman Award for his textbook on electromagnetics and RF integrated circuits. He was also a co-recipient of the 2013 Jack Kilby Award for Outstanding Student Paper for his work on an efficient quadrature digital spatial modulator at 60 GHz, as well as many other outstanding awards.

Panelist

Adeel Ahmad
Radar Systems Algorithm Engineer
Texas Instruments Inc.

BIO: Adeel Ahmad received his PhD in electrical engineering from the University of Illinois at Urbana-Champaign in 2014. He is currently working as a radar systems algorithm engineer in the mm-wave sensors group where he develops signal processing techniques for various automotive and industrial applications of mm-wave sensors. He holds multiple patents and has published more than 25 publications in academic journals and conferences.

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Panelist

Murtaza Ali
Vice President of Systems Engineering
Uhnder Inc.

BIO: Murtaza Ali is vice president of systems engineering at Uhnder Inc, where he oversees the development of radar systems. He has more than 25 years of experience in systems development. His current research focus is on radar signaling techniques, MIMO methods for imaging radars and interference mitigation/avoidance. Ali holds a PhD degree in electrical engineering from the University of Minnesota. He has 50+ U.S. patents and has published over 40 papers in refereed and invited forums. Ali is a senior member of IEEE.

Panelist

Dave Copps
CEO
Worlds

BIO: Dave Copps is known locally and internationally as a futurist, technologist and visionary regarding the roles that emerging technologies will play in transforming markets and the world. Dave has founded, launched and sold two technology companies that have placed machine learning and artificial intelligence in hundreds of companies around the world. In 2017 Copps was recognized as Emerging Company CEO of the Year in Texas while serving as CEO of Brainspace Corporation which was acquired by Cyxtera in 2017. Copps received his BA from the University of North Texas. He is an invited member of the Aspen Institute's Roundtable on AI, a frequent speaker at MIT's EmTech conferences as well as universities and technology incubators all over the world including Capital Factory, Health Wildcatters and the Dallas Entrepreneurs Center (The DEC) in his home town of Dallas, Texas.

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Panelist

Jianming Ma
Director
Texas Dept. of Transportation

BIO: Jianming Ma obtained his PhD degree in civil engineering from the University of Texas at Austin in 2006. As traffic management section director of the Texas Department of Transportation (TxDOT), Ma oversees the development of statewide traffic management programs including intelligent transportation systems (ITS), traffic signals, transportation systems management and operations (TSMO) and traffic incident management. Ma has over twenty-seven years of progressive experience in research, contract management and project and program management with a record of establishing operational optimization, developing high-performing teams and improving processes and procedures. Ma coordinates national research studies promoted by the American Association of State Highway and Transportation Officials (AASHTO) and the Transportation Research Board (TRB). The range of topics includes connected and automated vehicles (CAV), econometric modeling, human factors, ITS, systems engineering, traffic safety and transportation planning. He has authored, co-authored or contributed to about 50 technical papers and reports. Ma serves on the editorial board of the Journal of Safety Research.

Ma currently serves on the Board of the Transportation and Development Institute (T&DI) of the American Society of Civil Engineers (ASCE). He is the founding co-chair of the ASCE T&DI CAV Impacts Committee. He serves as a practitioner advisor for the Texas State University ASCE Student Chapter. Other national and international involvement activities include members of the TRB Committee on Traffic Signal Systems (ACP25). Ma is research development and implementation coordinator for the AASHTO Committee on Transportation System Operations. He has been invited to serve on numerous research panels related to transportation systems.

Panelist

Matt Markel
VP of Radar Systems
Ghost Autonomy

BIO: Matt Markel leads the radar systems division of Ghost Autonomy, an autonomous driving company using breakthroughs in collision avoidance technology to develop safe, attention-free self-driving for mass market consumer cars. His team is a diverse, innovative and collaborative group of electrical, mechanical, software and RF engineers with backgrounds from the tech, autonomy and defense sectors. He is also the editor and co-author of the widely lauded book "Radar for Fully Autonomous Driving."

Before Ghost Autonomy, he led the radar team at Waymo, formerly the Google Self-Driving Car Project. His radar department designed and delivered multiple generations of indigenously designed tracking and imaging radars to Waymo's self-driving fleet. He developed the radar research and development framework that has provided numerous cutting-edge technologies and capabilities to Waymo's radar product line.

At Raytheon, Markel was a Principal Engineering Fellow on the Space and Airborne Systems Technical Staff. He served as the technical director for Raytheon Advanced Electronic Warfare (EW), has been directly involved in the transition of key radar and EW capabilities to the U.S. military and has been a principal investigator for multiple radar and EW research programs that advanced the state of capability, effectiveness, autonomy and cognition in U.S. systems.

Markel is widely recognized as an expert and leader in radar, especially automotive radar for autonomous systems, Technology Readiness Assessments, Technology Readiness Levels (he served on the U.S. Government Accountability Office (GAO) panel of subject matter experts) and electronic warfare. He has multiple patents and trade secrets from his time at Raytheon and Waymo.

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10:50 a.m. CDT

Panelist

Balazs Simacsek
Director
Head of Hardware Security Architecture
NXP Semiconductors

BIO: Balazs Simacsek is the director of hardware security architecture in NXP´s Competence Center for Crypto and Security, where he leads the security architecture definition of microcontroller- and processor-based security solutions for different automotive, industrial and IoT applications. Before his current assignment, Simacsek was director of automotive security in NXP's automotive microcontrollers and processors business line, where he focused on the connectivity, ADAS, powertrain and vehicle dynamics, body and comfort domains. He also worked in NXP´s smart card business, developing high-security solutions for payment and secure identity applications.

Before that, he held various management and technical expert positions in the telecommunications and semiconductors industries.

He received his MS degree in electrical engineering and informatics from the Budapest University of Technology and Economics.

Panelist

Franklin Trujillo
Head of Technical Program Management for Product Infrastructure
Waymo

BIO: Franklin Trujillo is head of technical program management (TPM) for product infrastructure at Waymo, an autonomous driving technology company with a mission to make it safe and easy for people and things to get where they're going.

In this role, Trujillo leads Waymo's TPM team focused on scaling and commercializing the Waymo Driver. He works across multiple functions, including product, engineering, operations, marketing and regulatory, to ensure successful product launches across multiple markets. Having joined Waymo in 2020, he was part of several of Waymo's notable launches including the recent fully autonomous ride-hailing that was introduced to downtown Phoenix and San Francisco.

He has over twelve years of experience driving critical programs and product launches. Before Waymo, he was the lead technical program manager at Lyft, working on rider and driver apps and services. Before that, he was technical program manager at Google Nest and started his career as a business analyst then technical program manager at Cisco Systems.

Trujillo earned his bachelor's degree in business administration focused on information systems and computer science at California Polytechnic State University, San Luis Obispo. In his free time, he likes to run, climb and play volleyball. He is an avid traveler and foodie.

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LUNCH TALK: **Going Full Circle from Academia to Startup, Exit and Then Back at It Again**

12:30 p.m. CDT

Arjang Hassibi
Co-founder and CEO
Siomyx Inc.

ABSTRACT: Starting a company based on one's academic research is a daunting task. It requires not only the transfer of cutting-edge technologies out of a pure research environment into a rigid and structured development process but also the evolution of academicians into corporate (and business) superstars. Every startup has its own story, and every industry has its unique perks. However, there are many similarities between all academic startups. This talk attempts to go through some of them and highlight the challenges and discuss the fun parts.

In the beginning, we will talk about the early stages, incorporation and transition process for the core team. Next, we will discuss the product development stage and when the core team must facilitate growth and allow the company to evolve into a business. Finally, we briefly discuss exit scenarios and what will be next for the now "experienced" entrepreneurs.

BIO: Arjang Hassibi received the BS degree with the highest honors from the University of Tehran in 1997 and the MS and PhD degrees in electrical engineering from Stanford University in 2001 and 2005, respectively. He had his postdoctoral training at the California Institute of Technology.

He is currently the CEO of Siomyx Inc., a start-up company that he founded in 2022. Before that, he was The Founder and CEO of InSilixa Inc., a CMOS biochip company that was acquired by Danaher (Cepheid) Corp. in 2021.

He also has held various research and development positions in industry and academia, including serving as a professor at the Department of Electrical and Computer Engineering at The University of Texas at Austin, a research scientist at the Stanford Genome Technology Center and the CMOS High-Speed Integrated Circuits (CHIC) Laboratory at Caltech, visiting professor at IBM Research at Yorktown and co-founder and VP of engineering at Xagros Genomics. His areas of interest and expertise include the intersection of biotechnology and engineering, specifically biosensors and bioelectronics, molecular diagnostics, DNA sequencing and integrated sensors.

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INVITED SPEAKERS: Mars Helicopter Communication Link and Innovative Antenna for Cubesats, Landers and Rovers

3:20 p.m. CDT

ABSTRACT: Recent progress on antenna design and propagation modelling for space exploration, including antenna designs and propagation on the Mars surface, will be discussed and illustrated through a wide range of successful NASA missions.

NASA's Jet Propulsion Laboratory has developed the first Mars helicopter: Mars Ingenuity. The helicopter can transmit data from a Mars Rover up to 1 kilometer. After multiple successful flights, our team collected enough data to compare the accuracy of our models accounting for the shadowing effect, multipath, polarization loss and fading. This required highly accurate modeling of the Mars Rover and helicopter.

The second part of the presentation will discuss recent progress on antennas for Cubesats. NASA's Jet Propulsion Laboratory has significantly contributed to the rapid growth of CubeSat antennas with the development of deployable antennas at X- and Ka-band. This presentation will also cover technology development for future missions covering larger mesh reflectors and metasurface antennas.

Nacer Chahat
Senior Antenna/Microwave Engineer
NASA Jet Propulsion Laboratory

BIO: Nacer Chahat received the master's degree in electrical engineering from the Ecole Supérieur d'ingénieurs de Rennes (ESIR), France and the master's degree in telecommunication and a PhD degree in signal processing and telecommunications from the Institute of Electronics and Telecommunications of Rennes (IETR), University of Rennes 1, France. He is a senior antenna/microwave engineer with the NASA Jet Propulsion Laboratory (JPL) where he has been a technical section staff and product delivery manager since 2017. He wrote the textbook entitled CubeSat Antenna Designs describing work on CubeSat antennas developed at JPL. He is co-inventor of the iconic deployable reflectarray used on the Mars Cube One (MarCO) mission, the world's first interplanetary CubeSat. He also co-invented the award-winning Raincube mesh reflector antenna used on the first active radar on a CubeSat as well as the Europa Lander antenna. Chahat has received numerous awards including the NASA Early Career Achievement Medal Award in 2018 and the 2020 IEEE Outstanding Engineer of the Year from IEEE Region 6. In 2022, he received the Dr. Sudhakar Rao award, and he became a Fellow of the IEEE.

Gaurangi Gupta
Postdoctoral Researcher
NASA Jet Propulsion Laboratory

BIO: Gaurangi Gupta is a postdoctoral researcher at the NASA Jet Propulsion Laboratory (JPL) at the California Institute of Technology. She is currently working on antenna development for radio telescope and satellite communication applications. She completed her master's and PhD in electrical engineering from the Indian Institute of Technology (IIT) Kanpur, India in 2014 and 2020, respectively. During her PhD, she worked on the design and development of low-profile antennas with meta-surface revflectors. She worked as a research associate at IIT Kanpur during 2020-2021, where she worked on phased array antennas for satellite on-the-move applications under an industry-collaborated project. Under the Indo-US Fellowship for Women in STEMM, she worked as a visiting scholar at the Remote Sensing Center at the University of Alabama from 2018 to 2019, where she contributed to the ongoing radar development. She has published multiple papers in journals and conferences and is a recipient of best paper awards and travel grants at IEEE conferences.

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CENTER OVERVIEW

4:05 p.m. CDT

Kenneth K. O
Professor, The Jonsson School
Texas Instruments Distinguished University Chair
Director, TxACE
The University of Texas at Dallas

BIO: Kenneth O received his BS, MS, and PhD degrees in electrical engineering and computer science from the Massachusetts Institute of Technology in 1984, 1984 and 1989, respectively. From 1989 to 1994, Dr. O worked at Analog Devices Inc. developing sub-micron CMOS processes for mixed signal applications and high speed bipolar and BiCMOS processes. He was a professor at the University of Florida, Gainesville from 1994 to 2009. He is currently the Director of the Texas Analog Center of Excellence, Texas Instruments Distinguished University Chair and professor of electrical engineering focusing on analog circuits and systems at The University of Texas at Dallas. His research group is developing circuits and components required to implement analog and digital systems operating at frequencies up to 40THz using silicon IC technologies.

Dr. O is the past president of the IEEE Solid-State Circuits Society. He has authored and co-authored ~290 journal and conference publications, as well as holding 15 patents. Dr. O has received the 2014 Semiconductor Research Association University Researcher Award. He is also an IEEE Fellow.

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Poster Session Proceedings

October 17, 2022

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TxACE Analog Symposium 2022

Poster Session Proceedings

October 17, 2022
The University of Texas at Dallas

LIST OF POSTER ABSTRACTS Poster

315 GHz Reflectarray Antenna Fabrication Using Spin-on Dielectrics

Farhat Abbas, Nishanth Virushabadoss, and Rashaunda Henderson

Email: farhat.abbas@utdallas.edu

Abstract 1- *Antennas with high gain are very important components for different applications including remote sensing, wireless communications, and radars. In recent years the rapid development of technologies in the terahertz (THz) spectrum have made it highly desired to build high-performance antennas to obtain increased gain, improved aperture efficiency, and low sidelobe levels. Many attempts are being made to design such antennas, which include the lens antenna, horn antenna, and reflectarray antenna. The reflectarray antenna provides more flexibility in controlling the aperture phase and can be useful for many applications. We propose a reflectarray antenna operating at 315 GHz using patch antenna unit cells. This poster will discuss the fabrication and characterization of an offset fed design. The reflectarray patches have been printed using cleanroom lithography processing in which the negative photoresist of SU-8 is the dielectric. SU-8 is a spin-on material and capable of multiple thicknesses as a function of spin-speed and material viscosity. A horn antenna is incorporated as a feed source for the fabricated structure to test the performance of the design.*

Reducing underkill using unsupervised machine learning-based method in Analog/RF IC Testing

V. Amritur Niranjan, D. Neethirajan, A. Nahar, D. Webster, Y. Makris

Email: vxa172230@utdallas.edu

Abstract 2- *Semiconductor manufacturers strive to maintain a balance between the reliability expectations of System on Chips (SOCs) and ensuring the overall cost of testing is low. Amongst manufacturers, there exists a strong desire to achieve minimal Defective Parts Per Billion (DPPB) as loss of yield is often exacerbated by the exponentially increasing complexity of devices in current technology nodes. Most semiconductor manufacturers balance the need for extensive testing and the additive overhead of test cost and test time associated with it, resulting in manufacturers having exceedingly optimistic device binning or insufficiently elaborate test programs. The aforementioned issues in high-volume manufacturing testing cause faulty or failure-prone ICs to be shipped out and increase the number of customer returns. We term this unfavorable test outcome as Underkill. To this end, we propose an unsupervised machine learning-based methodology to identify potential customer returns and thus reduce Underkill. Specifically, the proposed machine learning model captures any deviations in device behavior across different test insertions. Leveraging unsupervised machine learning models, we extract unique signatures from these devices and use Gaussian methods to learn from the distribution and identify one or more devices that may be a potential customer return(s). We employ our proposed approach on an industrial dataset provided to us by Texas Instruments. Our experimentation with the industrial dataset establishes effectiveness in correctly identifying devices with a higher probability of failure on-site.*

Early Anomaly Detection in AMS Circuits of Automotive SoCs via Unsupervised Learning

A. Arunachalam, A. Kizhakkayil, S. Kundu, A. Raha, S. Banerjee, R. Jin, F. Su and K. Basu

Email: arunachalamayush@utdallas.edu

Abstract 3- *Recently, there has been an extensive adoption of safety-critical applications in the automotive domain, which has laid emphasis on ensuring the functional safety of Electrical and/or Electronic (E/E) systems in automotive vehicles. Due to their advanced manufacturing nodes, parametric perturbations, environmental stress, etc., Analog and Mixed-Signal (AMS) circuits that constitute such systems are more liable to faults than their digital counterparts. Their continuous signal properties, however, enable early anomaly detection and provide an opportunity to facilitate the deployment of mitigation strategies in order to subvert eventual system failure. Towards this end, we propose a novel unsupervised machine learning-based early anomaly detection framework catered to automotive AMS circuits. The proposed approach involves the generation of a comprehensive anomaly training dataset in various circuit locations and components, feature extraction from observation signals, and clustering algorithms to enable anomaly detection. The anomaly detection performance is further improved and expedited by incorporating time series analysis. In this work, we consider two AMS circuits commonly present in automotive systems-on-chips as our case studies. Our experimental results demonstrate the effectiveness of our solution, furnishing up to 100% accuracy. Furthermore, the time series approach reduces the anomaly detection latency by 5X.*

Joint Doppler Frequency and Direction of Arrival Estimation for TDM MIMO Automotive Radars

A. B. Baral, M. Torlak

Email: ashwinbhobani.baral@utdallas.edu

Abstract 4 - *This work considers a novel approach to joint estimation of the velocity (or Doppler frequency) and Direction of Arrival (DOA) of targets by time division multiplexing (TDM) multiple-input multiple-output (MIMO) radars in automotive applications. The TDM MIMO radars create orthogonal probing signals (in time domain) by allocating a transmitter to a separate time slot. In this work, we consider a standard TDM MIMO radar to be the one where transmitters are activated sequentially according to their natural spatial order. The drawback of the standard TDM MIMO approach is the coupling of velocity and DOA information of the targets. The coupling reduces the unambiguous estimation interval of the Doppler frequencies of the targets by the number of transmit antennas being multiplexed. In this work, we propose a novel cost function to jointly estimate both the Doppler frequency and the DOA of each target by reinstating the reduced unambiguous Doppler spectrum interval. Our approach is generally applicable to solve the Doppler ambiguity problems associated with any colocated standard TDM MIMO radar. To confirm this, we present the simulation results that evaluate the performances of two widely deployed TDM MIMO radar antenna configurations: non-overlapped and overlapped arrays. Moreover, we derive the analytical expressions to study the statistical performance of the proposed method. The simulation examples are presented to verify the performance of the proposed method as well as the accuracy of the analytical expressions.*

Activation Functions for DW LIF Neurons

W. Brigner, N. Hassan, X. Hu, C. Bennett, F. Sanchez, C. Cui, A. Velasquez, M. Marinella, J. A. C. Incorvia, J. Friedman

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Abstract 5- *Complementary metal oxide semiconductor (CMOS) devices display volatile characteristics, and are not well suited for analog applications such as neuromorphic computing. Spintronic devices, on the other hand, exhibit both non-volatile and analog features, which are well-suited to neuromorphic computing. Consequently, these novel devices are at the forefront of beyond-CMOS artificial intelligence applications. However, a large quantity of these artificial neuromorphic devices still require the use of CMOS, which decreases the efficiency of the system. To resolve this, we have previously proposed a number of artificial neurons and synapses that do not require CMOS for operation. Although these devices are a significant improvement over previous renditions, their ability to enable neural network learning and recognition is limited by their intrinsic activation functions. This work proposes modifications to these spintronic neurons that enable configuration of the activation functions through control of the shape of a magnetic domain wall track. Linear and sigmoidal activation functions are demonstrated in this work, which can be extended through a similar approach to enable a wide variety of activation functions.*

Investigation and On-Board Detection of Gate-Open Failure in SiC MOSFETs

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Abstract 6- *Gate open failures in power semiconductor occur when gate bond wire cracks or lift off leading to the loss of gate control. In-molded devices, the failure mode may occur intermittently making it very challenging to analyze and detect. In this work, gate open failures are comprehensively investigated in the context of SiC-based discrete MOSFETs. To understand the possible mechanism behind gate-open failure, thermomechanical finite element analysis is performed on a high-fidelity model that shows interfacial shear stress at the gate-bond. Furthermore, a robust onboard technique for the reliable cycle-by-cycle detection of gate open faults is proposed. The proposed technique is experimentally verified for all possible fault scenarios and shown to detect faults as low as 150 ns. It is shown that compared to the traditional DESAT protection scheme, the proposed mechanism can prevent potential shoot-through events that may be caused by gate-open failure.*

Ultra Low Power Robust SAR ADC for PMCW Automotive RADAR

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Abstract 7- *Low power, high sample rate, moderate resolution ADCs are necessary for phase-modulated continuous wave (PCMW) radar. Although a SAR architecture would be suitable for this requirement, most prior works focus on the SAR core with little attention paid to peripheral circuits such as the input driver of the ADC. Relaxing the summing node in a bottom plate sampling network from being a hard ground is desirable as sizing down the summing node switch decreases parasitics on that node and results in some savings in driver power. The swing and distortion on the summing node, which is captured by the end of the sampling period, can be cancelled by treating it as a 'dynamic offset' of the comparator preamp, allowing for a 10x reduction in switch size without much linearity loss in behavior simulation. Additionally, a comparison delay based metastability detection circuit is used to help reduce metastability error while still providing a correct residue for the second pipelined SAR stage.*

Efficient Quantum Circuit Design with a Standard Cell Approach

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Abstract 8- *We design quantum circuits by using a standard cell approach. Standard cells are used to obtain a representation of the circuit before deciding to compile to either NISQ or surface code lattice surgery circuits. This approach can speed up the layout of circuits with a regular structure. Our approach to co-designing quantum circuits can be used to estimate the resources necessary for a computation without using complex compilation methods. We design standard cells to support two Toffoli gate decompositions and starting from a 3D design of a multiplication circuit, we present evidence that, compared to the existing quantum circuit compilers, our method achieves shallower 3D circuit (by at least 2.5x) and with fewer SWAP gates.*

On-Chip Markov Continuous Random Spread-Spectrum Modulation (RSSM) for Switching Power Circuits EMI Regulation

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Abstract 9- *As automotive industry advances towards high levels of electrification and autonomous driving, safety and reliability of the electronic systems have become the paramount design concerns. The ever-growing electronic devices and further integration of electronic system have led to a record high level of EMI interference between devices. To reliably support the growing power consumption of electronic systems within very limited vehicle space, the power delivery system must achieve high power density and suppress EMI at the same time.*

To suppress EMI noise, this work presents a gallium nitride (GaN) based switching power converter operating at 8.3MHz. It employs a Markov continuous random spread-spectrum modulation (RSSM) technique to spread EMI spectra almost uniformly, and thus attenuate peak EMI level effectively. On the other hand, a one-cycle ON-time rebalancing scheme is designed to stabilize the duty-ratio of the converter even if the switching frequency changes randomly, suppressing the output voltage jittering without influencing the EMI reduction by RSSM. A prototype was designed and fabricated using a 0.18-μm HV CMOS process. With ±10% modulation range of a nominal switching frequency of 8.3 MHz, peak EMI is reduced from 66 to 35 dBμV at the fundamental frequency. In the meantime, the RSSM-induced output voltage jittering is suppressed from 240 to below 10 mV. The converter achieves a peak efficiency of 86.8% at 6.25 W.

AC Power Cycling Test Setup and Condition Monitoring Tools for High Power SiC Modules

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Abstract 10- *AC power cycling test allows more realistic reliability assessment by applying close to real stress to the device under test (DUT). This paper developed an AC power cycling test setup for high-power Silicon Carbide (SiC) modules. The suitable precursors for all dominant failure mechanisms are identified, and condition monitoring tools are designed to monitor the device's aging accordingly. The condition monitoring tools are combined with an in-built desaturation protection circuit of the gate driver to make them more practical and easier to implement with less no. of components. The on-resistance is selected as a temperature-sensitive electrical parameter to monitor the junction temperature of the device. Therefore, the phase currents and drain-to-source voltages of all DUTs are monitored online to measure on-resistance. To avoid heavy processing load, the out-of-order equivalent time sampling technique is used for data sampling. Following that, the sampled data is filtered by an FIR stage which leads to a measurement error of less than 1.5%. In addition, the design considerations regarding common mode noise and device parameters variation effect on the DESAT protection accuracy in a high-power setup are investigated in the experiment. Finally, the experimental results show the efficacy of the condition monitoring circuits and test setup.*

IHP SiGe HBT's for Power Amplification at 280 GHz.

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Abstract 11*- Our objective is to generate >10 dBm power at 280 GHz in IHP 130nm SiGe BiCMOS process. To achieve that, we used a 4-stage PA chain with a 4-way power combining at the output. The PA uses the Cascode topology with feedback capacitance between the input of C.E. stage and the output of C.B. stage. A T-shape matching network was used for interstage matching. A 4:1 combiner based on sub-quarter wavelength three-conductor transmission line baluns is used at the output. The design achieves a Psat of 10.7 dBm and a gain of 21 dB at 272 GHz in simulations. The PA will be integrated with a mixer in the same process and used to up-convert the output of a 140-GHz CMOS modulator to generate 10-dBm 280-GHz 64-QAM signals.*

140-GHz 60-Gbps 64/32/16-QAM Modulator with Programmable Supply Modulation in 65-nm CMOS

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Abstract 12- *A 140GHz 60-Gbps 64/32/16-QAM compatible modulator is designed in 65-nm CMOS process. On chip 10-GHz clock rate PRBS-11 is integrated as the data source for the QAM modulator measurement. 140-GHz on-chip injection locking QVCO is integrated to generate I/Q LO signal. Two BPSK modulators are employed for I and Q channel phase modulation, respectively. Amplitude modulation is implemented by modulating the current DAC. 48-bit RAM is implemented with DFFs to program the amplitude modulation power. Two path phase modulation and programmable supply modulation are combined by a Wilkinson combiner. The peak RF output power is 8 dBm.*

Energy efficiency challenges for all-spin logic

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Abstract 13- *As complementary metal-oxide semiconductor (CMOS) technology scaling reaches its limits, new compute-in memory technologies such as "all-spin logic" (ASL) are being explored. Preliminary predictions indicate that ASL implemented with perpendicular magnetic anisotropy will exhibit power-delay product (PDP) and energy-delay product (EDP) compared to CMOS, supporting its candidacy as a replacement for CMOS. In recent evaluations of ASL, unrealistic parameters have been used, leading to overly-optimistic efficiency figures. This paper uses micromagnetic simulations with realistic parameters to analyze the relationships between the various device parameters and circuit parameters, and the resulting impact on PDP and EDP. This analysis indicates that the PDP and EDP of ASL is greatly inferior to CMOS with the technological parameters that are currently available. In order to overcome these challenges relating to energy efficiency, this paper also evaluates the potential to modify the device parameters to improve the energy efficiency.*

Bridging the Gap Between 2-way and 1-way CSI-Based Ranging

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Abstract 14- *In today's wireless networks, localization is gaining increased importance due to the numerous location-based services in healthcare, logistics, and security expected to be provided by these networks and their future generations. A key element of the localization process is distance estimation (also known as ranging). In this work, we design and analyze efficient super-resolution decimeter-level 2-way ranging scheme for ubiquitous Wi-Fi networks in 5 GHz frequency band.*

We investigate the idea of channel frequency response (CFR) stitching and how 2-way CFR measurements help achieve CFR coherency that is necessary for accurate ranging. We also quantify the ranging accuracy degradation of 2-way compared to 1-way due to doubling multipath spread. We design a novel scheme to bridge the performance gap between 1-way and 2-way ranging which operates in three main steps: square-root of the 2-way CFR, phase unwrapping, then deep fade detection and phase errors correction. The proposed scheme was tested using an advanced Wi-Fi simulator incorporating accurate indoor wireless channel models. Our proposed scheme was shown to achieve significant performance gains over 2-way ranging with only a slight performance gap from 1-way ranging. The proposed scheme enjoys robustness as it preserved the ranging accuracy gains in various communication scenarios where we operate at different SNR levels and channel models while using different CFR bandwidth and number of receive antennas.

Phase Noise Reduction in LC VCO's Using an Array of Cross-Coupled Nano-Scale MOSFETs and Intelligent Post-Fabrication Selection

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Abstract 15- *The low frequency noise, thermal noise and DC characteristics of nano-scale MOS transistors with dimensions close to the process minimum are highly variable. This paper demonstrates a phase noise reduction technique in LC Voltage Controlled Oscillators (VCO's) by post-fabrication selection of a subset of an array of near minimum-size cross-coupled transistor pairs with reduced low frequency noise and thermal noise. Using an intelligent post-fabrication selection process, the phase noise is lowered from the maximum by 3.5 dB at 600-kHz, 1-MHz, and 3-MHz offsets from a 3.8-GHz carrier. The lowest phase noise of -122 dBc/Hz, -129 dBc/Hz, -139.5 dBc/Hz at 600-kHz, 1-MHz, and 3-MHz offsets, respectively from a 3.8-GHz carrier has been measured using the PLL method in Keysight E5052B Signal Source Analyzer. The VCO prototype was fabricated in a 65-nm CMOS process and dissipates 7 mW of DC power. The maximum figure of merit (FoM) including phase noise, carrier frequency and power consumption is 193 dBc/Hz and the figure of merit including the VCO core area, FoMA is 209 dBc/Hz.*

Slot Bow-Tie Antenna Integrated in Flip-Chip and Embedded Die Enhanced QFN Package for mmWave Applications

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Abstract 16- *Demand for compact and miniaturized millimeter-wave (mmWave) front end modules is driving research in planar antenna integration along with other mmWave components into a package. These solutions support industrial wireless applications and future 6G technology. This poster presents two innovative antenna-in-package (AiP) integration technologies in quad flat pack no-lead (QFN) format. A slot bow-tie (SBT) antenna designed for WR8 (90GHz-140GHz) and WR5 (140GHz-220GHz) frequency bands is integrated for the first time into flip-chip enhanced QFN (FCeQFN) and embedded die enhanced QFN (EDeQFN) package technologies. A brief description of designs, modeling methodologies and simulation results of mmWave chip-to-package transitions, transmission line structures, and antenna feed elements are provided. The insertion and return losses of these structures are simulated and found to be less than 1.07dB and greater than 17dB, respectively for the FCeQFN package. In the case of the EDeQFN package, the insertion and return losses are observed to be less than 0.87dB, and greater than 22dB, respectively. The observed bandwidths in the WR8 and WR5 bands for the SBT antenna in both package types are 40GHz and 80GHz with a peak gain of 7dBi and 7.5dBi, respectively. The design of multiple test vehicle structures and a novel measurement methodology for antenna-in-package bandwidth, and radiation pattern characterization in the WR5 frequency band is also presented in this poster.*

Genetic Physical Unclonable Functions in Human Cells

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Abstract 17- *A Physical Unclonable Function (PUF) is a physical entity which provides a measurable output that can be used as a unique and irreproducible identifier for the artifact wherein it is embedded. Popularized by the electronics industry, silicon PUFs leverage the inherent physical variations of semiconductor manufacturing to establish intrinsic security primitives for attesting integrated circuits. Owing to the stochastic nature of these variations, photo-lithographically manufactured silicon PUFs are impossible to reproduce (thus unclonable). Inspired by the success of silicon PUFs, we sought to create the first generation of genetic physical unclonable functions in human cells. We demonstrate that these PUFs are robust (i.e., they repeatedly produce the same output), unique (i.e., they do not coincide with any other identically produced PUF), and unclonable (i.e., they are virtually impossible to replicate). Furthermore, we demonstrate that CRISPR-Engineered Physical Unclonable Functions (CRISPR-PUFs), can serve as a foundational principle for establishing provenance attestation protocols.*

Cross-Point Metal-Ferroelectric-Metal Capacitors Array Devices for Neuromorphic Computing Applications

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Abstract 18- *Beyond the scaling down challenges on the memory devices, significant efforts have been devoted to the advancement in artificial neural networks (ANNs) in order to achieve low power-consumption and high computing efficiency. As the adoption of ferroelectricity in the ANN systems, most researchers have demonstrated the ferroelectric field-effect-transistors (FEFET) based vector-matrix multiplication (VMM) which can optimize the analog conductance states. In this work, we demonstrate the 2×2 pattern recognition using a simple cross-point array of MFM capacitors. Such MFM capacitors enable the memory behaviors defined by the amount of stored charge, which is measured by an electrical signal such as a current or a voltage. The fabricated devices exhibit an excellent reproducible operation in device-to-device variation, enabling the outstanding vector matrix multiplication (VMM) eligible for the neuromorphic computing with a binary weight. As the pattern recognition results, reading the charge signal as current signal have 81.3% of the recognition accuracy, while that as the voltage signal allow the 100% accuracy in the voltage-based operation. We thus believe that the promise of the simple MFM capacitors is eligible for the neuromorphic computing applications.*

Room Temperature and Elevated Temperature Measurements of CeRAM based RF Switches

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Abstract 19- *RF switches are extensively used in RF systems to route high frequency signals through different transmission paths. Figure of Merit (FOM=) is often used to compare the performance of RF Switches. It is highly desirable to minimize Ron and Coff to minimize insertion loss and maximize isolation. It is critical to accurately measure these parameters of on-wafer devices to obtain the correct FOM. Here we are presenting a novel Correlated Electron (Ce) switch that is not only capable of performing at tens of THz regime but can work at Ultra-high-temperatures (>200. The RF testing is done at Texas Analog Center of Excellence (TxACE). The primary equipment for RF testing is an Agilent PNA-X network analyzer, with a switching operation test done with Agilent 4155C Semiconductor Parameter Analyzer. In addition to structures with RF switch, we also have on-wafer open and short structures to de-embed the bond-pad and series interconnects. Both Ron and Coff are obtained using the measured Z-parameter of the DUT, on-wafer open and short structures and performing open-short de-embedding. Ron is measured using the Z-parameters of the DUT in the SET state. Coff is measured using the Z-parameters of the DUT in the RESET state. We perform these measurements at both room temperature and 125 to make sure that the switch works at high temperatures. 250 ℃ testing is also planned in the future.*

A Wide Bandwidth GaN-Based Power Amplifier for IR-UWB Front End Transmitter System for Far-Field Wireless Power Transfer Applications

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Abstract 20- *One of the most crucial aspects of developing a pulse-based WPT system for drone-to-drone charging is the design of an efficient power amplifier. To achieve a high-power transfer efficiency from the transmitter (TX) antenna to the receiver (RX) antenna, it is imperative to design a power amplifier that can deliver a high output power and achieving a high power-added efficiency (PAE). Thus, an efficient design approach is required that considers the proper selection of the transistor, load-pull analysis, and proper input and output matching network design strategies for achieving the ultra-wideband frequency range of operation. This paper presents the design of an ultra-wideband power amplifier (PA) that can operate in the 6 -8.5 GHz ultra-wideband (UWB) frequency range. The Qorvo TGF2977 GaN HEMT model is used for the design of this power amplifier since this transistor can operate up to 12 GHz frequency thus covering the ultra-wideband frequency range (3.1 – 10.6 GHz). The design approach includes obtaining the optimum operating conditions for the transistor and to find the optimum load and source impedances to design the input and output matching networks. The input and output matching networks are designed with the goal to achieve a wide bandwidth. The optimized design of the input matching network can make the PA achieve an ultra-wideband frequency from 1.76 – 7.53 GHz thus achieving an ultra-wide bandwidth of 5.77 GHz. The PA achieves the highest output power of 32.8 dBm for an input power of 17 dBm thus yielding the highest gain of 15.8 dB at the 6 GHz frequency. The PA proposed in this work has a higher gain and a higher bandwidth compared to prior works. Future works are going to include achieving a higher bandwidth while also achieving a higher output power, gain, and PAE over the whole bandwidth by changing the matching network topologies and optimizing the component parameters to achieve the desired goal.*

Design and Testing Methodology for Broadband Antennas in Package Operating in the WR8 and WR5 Frequency Bands

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Abstract 21- *Broadband millimeter-wave (mm-wave) antennas-in-package (AiP) are challenging to design due to their surrounding environment. Several factors the AiP designer needs to consider are over mold thickness, feed losses and direct electromagnetic (EM) effects to the antenna radiation pattern. In particular, EM effects due to proximity of a silicon die containing active circuits need to be considered. This paper presents the antenna selection process rationale and the design process of E-shaped patch and slot bowtie antennas in the WR8 (90-140GHZ) and WR5 (140-220GHz) bands integrated on an enhanced QFN package. Pros and cons for each integrated AiP will be discussed. Moreover, the standalone antenna including an over molded protective dielectric is compared against the fully integrated AiP will be presented. Performance comparisons are made by observing the radiation pattern characteristics, efficiency and -10dB input impedance bandwidth. To validate the simulation results of the AiP, a test vehicle containing the WR5 slot bow tie antenna has been designed and is currently being manufactured. A brief discussion of the testing methodology for this AiP test vehicle will be introduced as part of this continuous research.*

Analog Memory Trimmed Switch Mode Regulator

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Abstract 22- *We present an analog integrated circuit which uses analog programing for precision regulation of a switch-mode regulator. The analog trimmable switch-mode regulator is a buck regulator, which is ubiquitous in the industry. Typically, such a regulator is trimmed for improved accuracy and flexibility, usually using a combination of digital trim and design-to-target specifications. Here we have a design that does not have digital trim capability and uses analog trim. The analog input voltage to the buck regulator is 3.3V and its output voltage is trimmable around 1.8V. The buck regulator power switch is a PMOS, and it consists of a control circuitry which includes an opamp voltage feedback, oscillator and switching logic, a startup circuitry to avoid startup voltage overshoot and a current limit circuitry. Trim for currents, voltages, current limits and oscillator frequency are provided from the analog memory cells. The analog memory cells consist of a capacitor which can be charged and discharged through tunnel junctions.*

Adaptive V_{min} Seed Forecasting for Fast Calibration using Inter-V_{min} Correlation

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Abstract 23- *High-performance mobile devices have limited power sources and hence, functioning at low power levels is an important constraint for their success. Process variation causes such critical specification parameters of high-performance devices to deviate from their ideal performance. Hence it is necessary to use post-silicon calibration to identify the minimum operating voltage (V_{min}) for a device. The device under study has the capability to operate at four different speeds. Hence, the device has four different V_{min} values that have a linear relationship to the speeds associated with it. Recent studies have shown that the current V_{min} search can be improved by modeling the starting point of the search as a function of the e-test signatures per wafer. In this paper, we expand on the V_{min} search calibration seed forecasting by taking advantage of the relationship between the different operating voltages for the Device Under Test (DUT). The proposed method predicts the starting voltage of the search and the highest possible voltage level as a function of the other operating voltages associated with the device. The effectiveness of the proposed methodology is demonstrated on an industrial dataset provided by Texas Instruments.*

Reduced-Complexity Decimeter-Level Bluetooth Ranging in Multipath Environments

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Abstract 24- *Distance estimation (also known as ranging) is a highly desired function for localization as it enables new services like asset tracking, commissioning of sensors, keyless entry systems, and many more. In this work, we investigate enhanced super-resolution range estimators with decimeter-level accuracy for multi-antenna and multipath Bluetooth systems. To enhance traditional ranging using the classical MUSIC algorithm for two-way frequency-hopping Bluetooth transmissions, we apply forward-backward averaging and bandwidth extrapolation using Burg's linear predication algorithm to improve ranging accuracy, which is limited by the used Bluetooth bandwidth and the quality of the estimated sample covariance matrix. For the multiantenna case, we compare the Summed Antenna Processing and Individual Antenna Processing methods to process multiple-antenna Bluetooth channel measurements and enhance ranging accuracy compared to the single-antenna case. In addition, we investigate sparsity-aware ranging which exploits the sparsity of Bluetooth channel impulse response and achieves comparable ranging accuracy to the enhanced MUSIC estimator but at a much lower computational complexity. We apply the greedy Orthogonal Matching Pursuit algorithm to heuristically solve the sparsity-constrained optimization problem for Bluetooth ranging. Furthermore, we evaluate the computational complexity of our investigated Bluetooth ranging with two complexity-reduction techniques to further reduce the complexity of MUSIC ranging. Finally, we evaluate the Root-Mean-Square Error and Empirical Cumulative Distribution Function performance of our investigated range estimators both on simulated and real-world Bluetooth data that we collected in line-of-sight (LOS) and non-line-of-sight (NLOS) multipath scenarios. Our proposed ranging enhancements improved the ranging accuracy by 58% for our collected Bluetooth data.*

A Four Channel Impulse Radio Ultrawideband (IR-UWB) Front End Transmitter System for a 2 × 2 Quadrature Based Phased Array Antenna Designed in 180 nm CMOS Process

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Abstract 25- *One of the challenges of integrating phased array antennas with an IR-UWB transmitter system is to transmit impulse signals at various phases to achieve different beam steering angles and transmit the highest possible power efficiently to the antenna arrays to enhance the gain of the antenna. Prior works that demonstrated wireless power transmission schemes using ultrawideband signals, were limited in terms of the transmitter system design along with the antenna design optimization to deliver the highest power and improve the PTE. To overcome these constraints, this paper presents the design of a four-channel IR-UWB transmitter system for a 2 X 2 quadrature phased array antenna using the standard 180 nm CMOS process. The system consists of a voltage-controlled ring oscillator (VCRO) which achieves a linear frequency range of 2.31 – 8.03 GHz by tuning the control voltage from 0.1 – 0.9 V. The designed impulse generator can generate as low as 435 ps impulse signal with 100 MHz pulse repetition frequency (PRF). The impulse is delayed by controlling the delay control voltages of the two double-inverter-based delay blocks thus achieving a delay range of 160 to 260 ps. The designed class-C power amplifier can deliver as high as 32.2 dBm output power at 3 GHz achieving a gain of 14.2 dB and a power added efficiency (PAE) of 50.1 %.*

Finger Regulated Simultaneous Noise and Input Matching Technique for a 2.4 GHz Low Noise Amplifier

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Abstract 26- *The objective of this work is to develop a finger-regulated simultaneous noise and input matching (FRSNIM) methodology for a 2.4 GHz ISM band Low Noise Amplifier (LNA). It is based on the principle of impedance settling of source referred noise impedances (Zopt) in order to achieve a theoretical optimization exploiting the Keysight's Advanced Design System (ADS) platform and the 180 nm standard CMOS process. The proposed FRSNIM mechanism takes into account the parasitics associated with the bond pad and bond wire to model the influence of the packaged parasitic on scattering port parameters. Exploiting the proposed FRSNIM scheme, the proposed LNA achieves 10.16 dB forward gain and 2.82 dB noise figure (NF) at 2.4 GHz, consuming only 8.5 mW of power with 1 V supply voltage, which makes it highly suitable for biomedical transceivers for implantable sensor applications.*

A Comparative Analysis of UWB Phased Arrays with Combining Network for Wireless Power Transfer Applications

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Abstract 27- *This article presents the theory, design, and demonstration of the performance of multiple ultra-wideband and low-profile modified microstrip line-based phased array antennas with 4 × 4 and 6 × 6 quadrants. A comparative analysis of the performance between 4 × 4 and 6 × 6 phased antenna arrays is demonstrated in terms of dimension, gain, half-power bandwidth (HPBW), and beam steering capability. The measured peak gains for the 4 × 4 and 6 × 6 antenna arrays are 12.11 dBi and 24.05 dBi, respectively, while also achieving an S11 <-35 dB and an axial ratio < 2 dB. The 4 × 4 array achieves a bandwidth (BW) of 0.69 GHz (6.42-7.11 GHz, fractional bandwidth (FBW) of 10.19%) while the 6 × 6 array achieves 1.67 GHz BW (8.93-10.60 GHz, 17.10% FBW). The measured radiation pattern of the 4 × 4 antenna array shows a beam steering range of -13° to 99° along the φ-axis and -9° to -81° along the θ-axis. The measured beam scanning performance of the 6 × 6 antenna array indicates a -150° to 30° steering range along the φ-axis and -15° to 45° along the θ-axis. The results demonstrate that the suggested antenna arrays are promising candidates for unmanned aircraft system (UAS) based wireless power transfer (WPT) systems.*

An Optimized Control System for the Independent Control of the Inputs of Doherty Power Amplifier

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Abstract 28- *The designed system enables independent control of the amplitudes and phases of the drive signals fed to the inputs of two parallel PAs that can be used in a Doherty PA architecture. This is achieved by incorporating a variable amplitude shifter (VAS) and a variable phase shifter (VPS) in each of the two parallel paths, which allows for driving uneven power levels with an arbitrary phase difference to the individual PAs. The specific VAS (Qorvo QPC6614) and VPS (Qorvo QPC2108) components that we used for the test system provide an amplitude attenuation range from 22 dB to 31.5 dB with a step size of 0.5 dB and a phase range from 0◦ to 360◦ at the intended operating frequency of 2.5 GHz, offering the benefit of characterizing the behavior of PAs under test for a large range of drive signals to optimize the output performance such as power added efficiency or adjacent channel leakage ratio. For demonstration, the proposed drive signal control system is integrated with two parallel GaN transistor-based PAs (Qorvo QPD0005) with a P1 dB of 37.7 dBm, whose output signals are combined and then measured to provide system characterization. Each PA is preceded by a drive amplifier with a gain of 17.8 dB to boost the power fed into the PA. The proposed circuit also incorporates a 20 dB directional coupler and a 3 dB Wilkinson power splitter, which were designed, fabricated on an FR4 substrate, and experimentally verified. While Qorvo QPD0005 was used as a specific test-case in this demonstration, the proposed system can be used to characterize the behavior of a wide range of Doherty PAs.*

Magnetic Sensor-based Automatic Beam Tracking system for 2.4 GHz Near-field Phased-Array based Wireless Power Transfer System in Neuromodulation Applications

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Abstract 29- *A magnetic sensor-based automatic beam tracking method is presented for a phased array-based wireless power transfer system to be implemented in neuromodulation applications. This method is proposed to track the position of the receiver (placed on the skull of a freely moving animal) and transmit the microwave signal with a focused beam to the target receiver. The coordinate locations of the target are obtained from the magnetic sensor and are converted into phase information for the instantaneous beam steering of the phased array. The system is constructed by a 2.4 GHz near-field 4×4 phased array transmitter antenna with four 4-bit phase shifters. The phased array TX antenna steers the beam from -5° to -155 in the θ plane. The magnetic sensor can detect the location of the receiver in this steering range. The process of tracking the target and focusing the beam has been evaluated by simulation.*

A Novel Method for Designing High Power Low Emittance DC Electron Gun with Numerical Methods and Image Processing

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Abstract 30- *Particle accelerators are machines that accelerate atomic or subatomic particles for a purpose. Particle accelerators in today's technology accelerate, direct and focus charged particles by electromagnetic forces. This technology finds dozens of application areas in many civil and military sectors and plays critical roles. Electron guns are being used widely in pre-accelerator of many applications. It provides proper accelerator fields that affect beam dynamics in the rest of the system. They are used in scientific instruments, electron devices, and industrial facilities. Although there are numerous design requirements changes depending on the application, the main challenge for DC electron guns is to achieve building high power together with low emittance electron beam. In this work, we present a novel method for designing high power low emittance DC electron gun with numerical methods and image processing. After determining electrode shapes of electron gun in Computer Simulation Technology (CST) to obtain desired parameters correlation, 2D electric field optimization of the electron gun is conducted via MATLAB by using finite difference numerical method. Image processing tool is used to transfer determined electrode shapes from CST to MATLAB. Since CST makes a 3D solution, simulation completion time takes a long time. Thanks to axially symmetrical structure of the electron gun, 2D solution gives results very fast and accurately to acquire design parameters. Optimization results in MATLAB are verified in CST as well, and final electrode structures are designed by attaining high power and low emittance electron beam.*

Defect Tolerance Framework from improving IC Yield

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Abstract 31- *In the latest technology nodes, there is a growing concern about yield loss due to timing failures and delay degradation resulting from manufacturing complexities. Largely, these process imperfections are fixed using empirical methods such as layout guidelines and process fixes which come late during the design cycle. In this work, we propose a framework for improving the design yield by synthesizing netlists with improved ability to withstand delay variations to reduce yield loss. We advocate a defect tolerant approach during early design stages to synthesize netlists by introducing defect-awareness to EDA synthesis, thereby generating robust netlists that can withstand delays induced by process imperfections. Toward this objective, we present a) a methodology to characterize standard library cells for delay defects to model the robustness of the cell delays, and b) a solution to drive design synthesis using the intelligence from the cell characterization to achieve design robustness to timing errors. We also introduce defect tolerance metrics to quantify the robustness of standard cells to timing variations, which we use to generate defect-aware libraries to guide defect-aware synthesis. Effectiveness of the proposed defect-aware methodology is evaluated on a set of benchmarks implemented in GF 12nm technology using static timing analysis (STA), revealing a ~75-85% reduction of yield loss due to timing errors arising from manufacturing defects, with minimum impact on the area, power and no impact on performance.*

Sleep Monitoring Using mmWave Radar Sensors

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Abstract 32- *The importance of the quality of sleep on our general wellbeing is well documented. However, longitudinal analysis of sleep is hindered by the fact that evaluation of sleep is restricted to clinical settings. In-home non-invasive methods of sleep data collection and evaluation is required to make sleep monitoring more ubiquitous and accessible to the broader demographic. Current research on non-contact methods of monitoring sleep can be divided into posture classification, sleep stage classification, and vital signs monitoring. The ability of mmWave sensors to detect large scale limb motion as well as micro motions due to breathing and beating of the heart make them promising candidates to achieve all three objectives. In this research, a comprehensive algorithm is presented to accomplish overnight monitoring of vital signs as well as sleep stage classification and generation of sleep metrics that provide insight into a number of sleep disorders. These are attained based on a single mmWave radar sensor, hence removing the need for multiple sensors. Real life experiments are conducted without any restrictions for monitoring sleep and promising results are obtained in comparison to a reference wearable device.*

A Software Defined Radio WiFi Localization Testbed

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Abstract 33- *Emerging localization solutions are difficult to test using off-the-shelf WiFi devices due to lack of customizability. Software defined radios (SDRs) offer programmable hardware for scalable prototyping of our own and emerging localization solutions. However, adapting such hardware to transmit and receive WiFi signals suitable for localization poses several challenges. Sub-nanosecond time synchronization is necessary between devices to allow for high accuracy localization. Moreover, hardware impairments including nonlinear filter effects, local oscillator phase offsets, and time offsets which affect the measured channel response need to be addressed. This work presents a testbed which addresses these impairments and offers multi-channel, multi-antenna, time synchronized timestamp and CSI measurements using WiFi signals for localization. The testbed utilizes Ettus X310 universal software radio peripherals (USRPs) with a National Instruments CDA-2990 clock distribution device for external time and frequency synchronization. In the practical case without external synchronization, we propose a two-way synchronization approach. The testbed supports measurements on all 2.4 GHz and 5 GHz WiFi channels with bandwidths up to 160 MHz. Transmissions used for ranging support the 802.11ac, 802.11ax, and legacy wireless standards in terms of preamble structure. Collection of measurements is simplified through a LabVIEW graphical interface with real-time visualization of measurements, and a MATLAB back-end is used for waveform generation, signal processing, and saving data for post processing. Using our testbed, we demonstrate centimeter-level maximum accuracy after calibration and decimeter-level accuracy in an indoor cluttered room environment with many multipath components.*

A Practical Switch Condition Monitoring Solution for SiC Traction Inverters

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Abstract 34- *As automotive manufacturers move towards Silicon Carbide (SiC) MOSFET based traction inverters, practical online switch condition monitoring solutions are crucial to address potential reliability concerns. In this work, an end-to-end practical online condition monitoring solution is proposed. An online sensing circuit is proposed which enables online on-state resistance (Rds-on) measurement for all six switches of the inverter. To address the challenge of periodic data acquisition alongside higher priority motor control tasks, a fast, code-efficient out-of-order equivalent time sampling technique is also proposed. The obtained periodic, high resolution Rds-on data is filtered by a Kalman filter stage. With the proposed measurement solution, Rds-on obtained at the motor current peak has an error of < 1.5%. Furthermore, the symmetrical nature of the inverter's operation is exploited to propose a Bayesian inference solution for independent online state-of-health (SoH) estimation for all six switches. This technique isolates aging related Rds-on change from operating conditions related changes. In particular, by automatically accounting for device and system level variations in the model, the proposed Bayesian SoH estimation solution eliminates the need for extensive system/device specific calibration. The efficacy and robustness of the proposed solution is tested by inducing bond-wire failure in several decapsulated discrete SiC MOSFETs.*

Design of Folded Reflectarray Antenna for THz Imaging Applications

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Abstract 35- *THz Imaging is an emerging method for non-destructive evaluation of materials. The imaging system typically requires a highly directive antenna (~40 dBi) to meet the resolution requirements. Reflectarray antennas are preferred because of its planar structure and ease of integration. This work will initially discuss about the traditional offset fed reflectarray antenna operating at 315 GHz. Next, we discuss about the design and measurement of Folded Reflectarray Antenna (FRA) operating at 410 GHz which will be integrated with the THz imaging system. The FRA topology doesn't have feed blockage like traditional reflectarray antennas. This work will also discuss in detail about the operation of the individual array element and the design of entire FRA. The work further discusses about the measurement technique that will be used to characterize the performance of the FRA.*

Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching

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Abstract 36*- The use of analog resistance states for storing weights in neuromorphic systems is impeded by fabrication imprecision and device stochasticity that limit the precision of synapse weights. This challenge can be resolved by emulating analog behavior with the stochastic switching of the binary states of spin-transfer torque magnetic tunnel junctions (STT-MTJs). This poster therefore describes a synchronous spiking neural network system with clocked circuits that perform unsupervised learning leveraging the stochastic switching of STT-MTJs, including simulations that demonstrate that this system enables a single-layer network to achieve 90% inference accuracy on the MNIST handwritten digit recognition task. Furthermore, we present the first experimental demonstration of a neuromorphic network with MTJ synapses, which performs image recognition via vector-matrix multiplication.*

430-GHz CMOS Concurrent Transceiver Pixel Array for High Angular Resolution Monostatic Imaging

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Abstract 37- *This work reports a prototype of a 430-GHz frequency-shift-keying (FSK) 1×3 concurrent transceiver (TRX) pixel array in a 65-nm CMOS process that can be used for high angular resolution monostatic imaging and ranging. The pixels integrate a transmitter, receiver, LO, and on-chip antenna into an area of 374×380 µm2. The pixels are 2-D scalable to increase its field of view (FoV). In RX operation, employing 3rd harmonic down-conversion, the pixel achieves a sensitivity of -102.5 dBm at 1-kHz bandwidth, which is the lowest among the 2-D scalable concurrent TRX pixels operating at frequencies near and above 300 GHz. Using the 3rd harmonic signal from a differential Colpitts oscillator, the total equivalent isotropic radiated power (EIRP) of the three pixels combined is −4 dBm at 430 GHz. With a 6-cm-diameter Cassegrain reflector, the EIRP is further boosted to 23 dBm and angular resolution is reduced to ~0.7°. The total DC power consumption of the entire chip is 165 mW. Out of which, 28.6 mW is dissipated in a single pixel including 4 mW for the integrated intermediate frequency LNA. Using the imager module, several experiments are demonstrated, including the lateral resolution test, imaging through heavy fog, and even a cardboard box.*